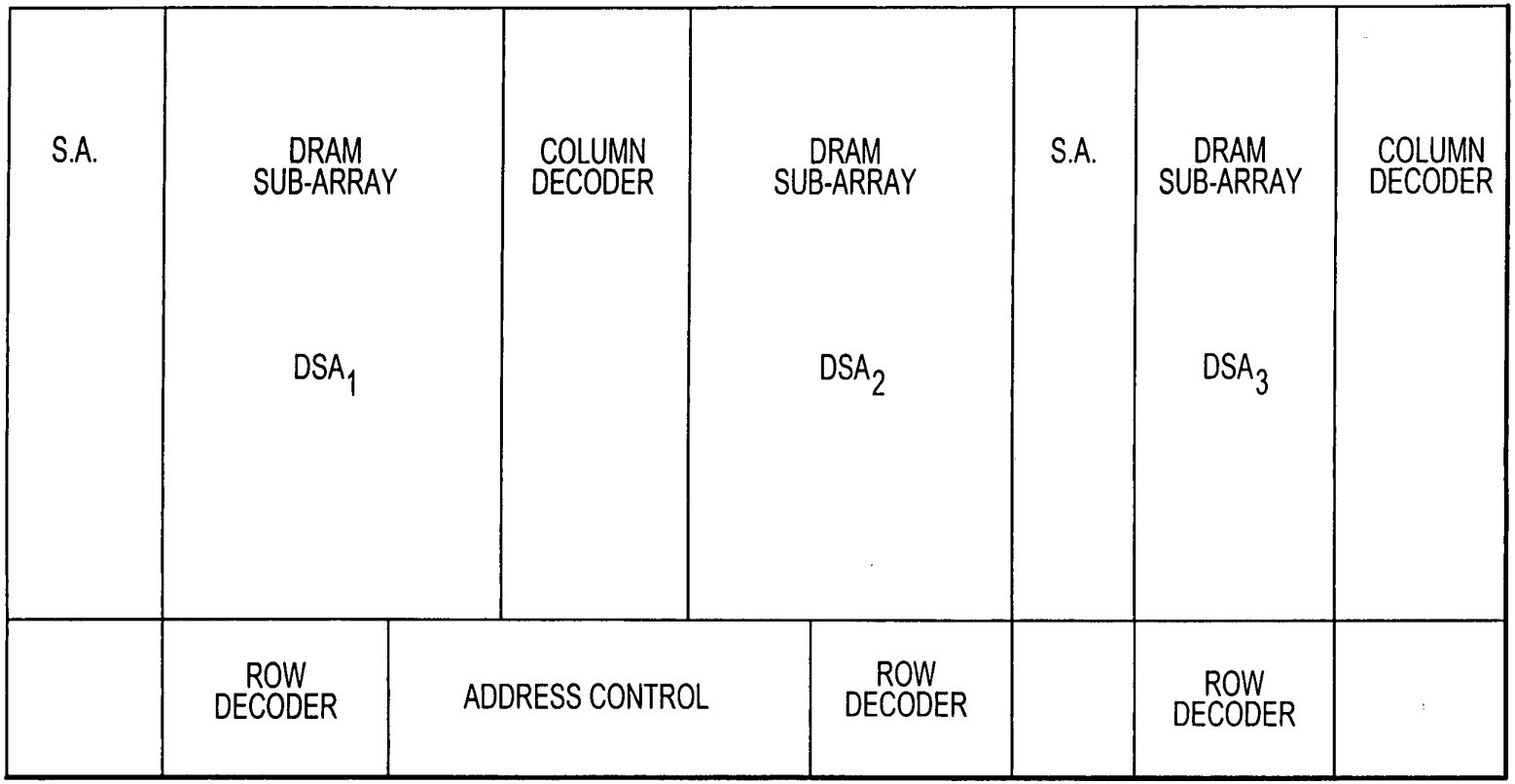

FIG.1A

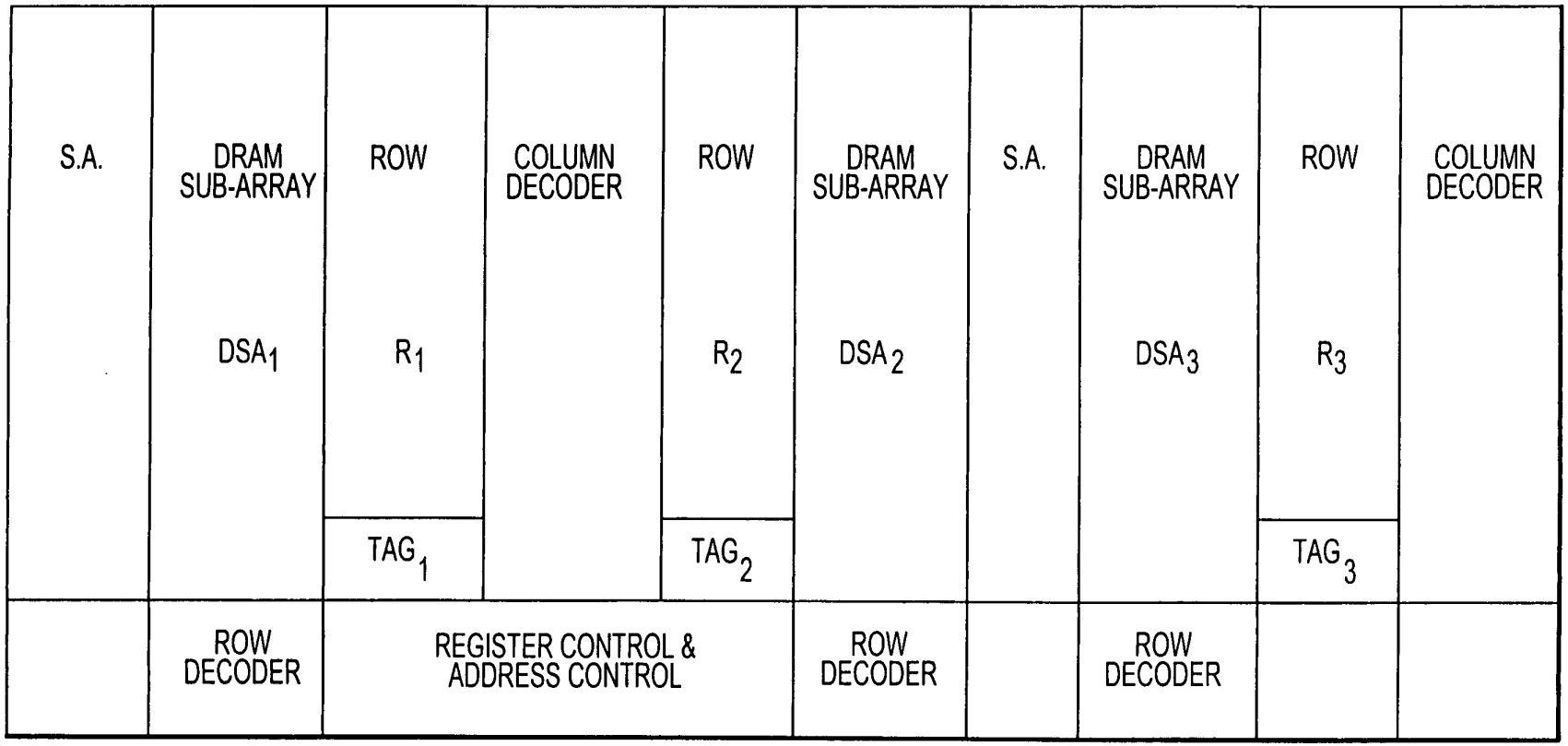
S.A.
DRAM SUB-ARRAY
DSA1
ROW
R1
TAG1
COLUMN DECODER
ROW
R2
TAG2
DRAM SUB-ARRAY
DSA2
S.A.
DRAM SUB-ARRAY
DSA3
ROW
R3
TAG3
COLUMN DECODER
ROW DECODER
REGISTER CONTROL & ADDRESS CONTROL
ROW DECODER
ROW DECODER

FIG.1B

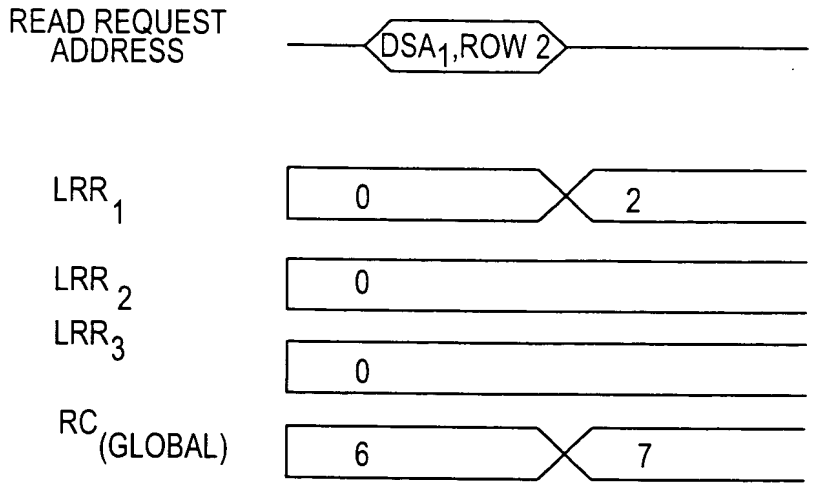
READ REQUEST ADDRESS
DSA1,ROW 2
LRR1
0
2
LRR2
0
LRR3
0
RC (GLOBAL)
6
7

FIG.2

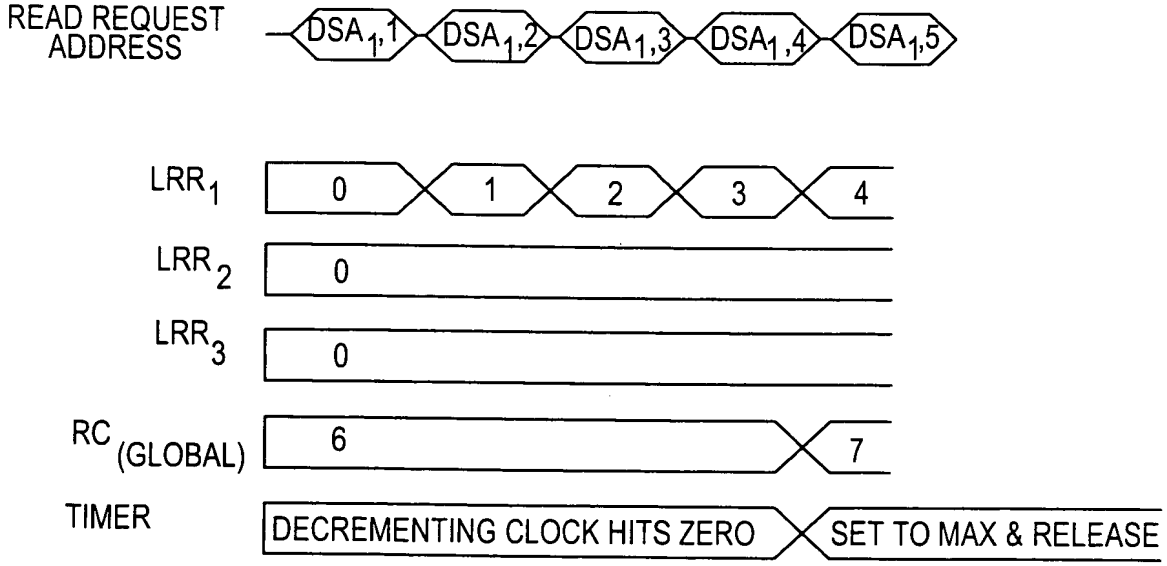
READ REQUEST ADDRESS
DSA1,1
DSA1,2
DSA1,3
DSA1,4
DSA1,5
LRR1
0
1
2
3
4
LRR2
0
LRR3
0
RC (GLOBAL)
6
7
TIMER
DECREMENTING CLOCK HITS ZERO
SET TO MAX & RELEASE

FIG.3

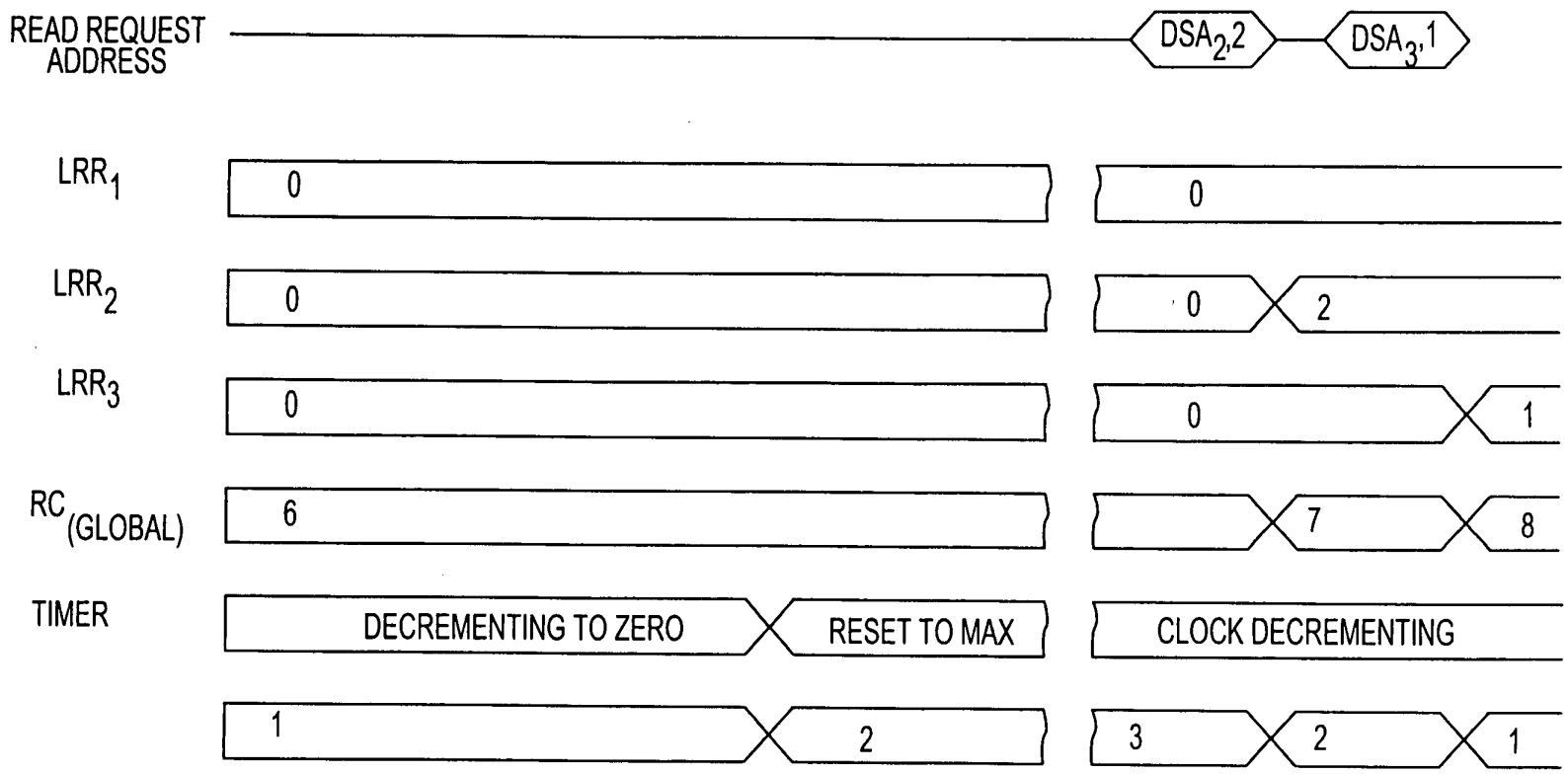

FIG.4

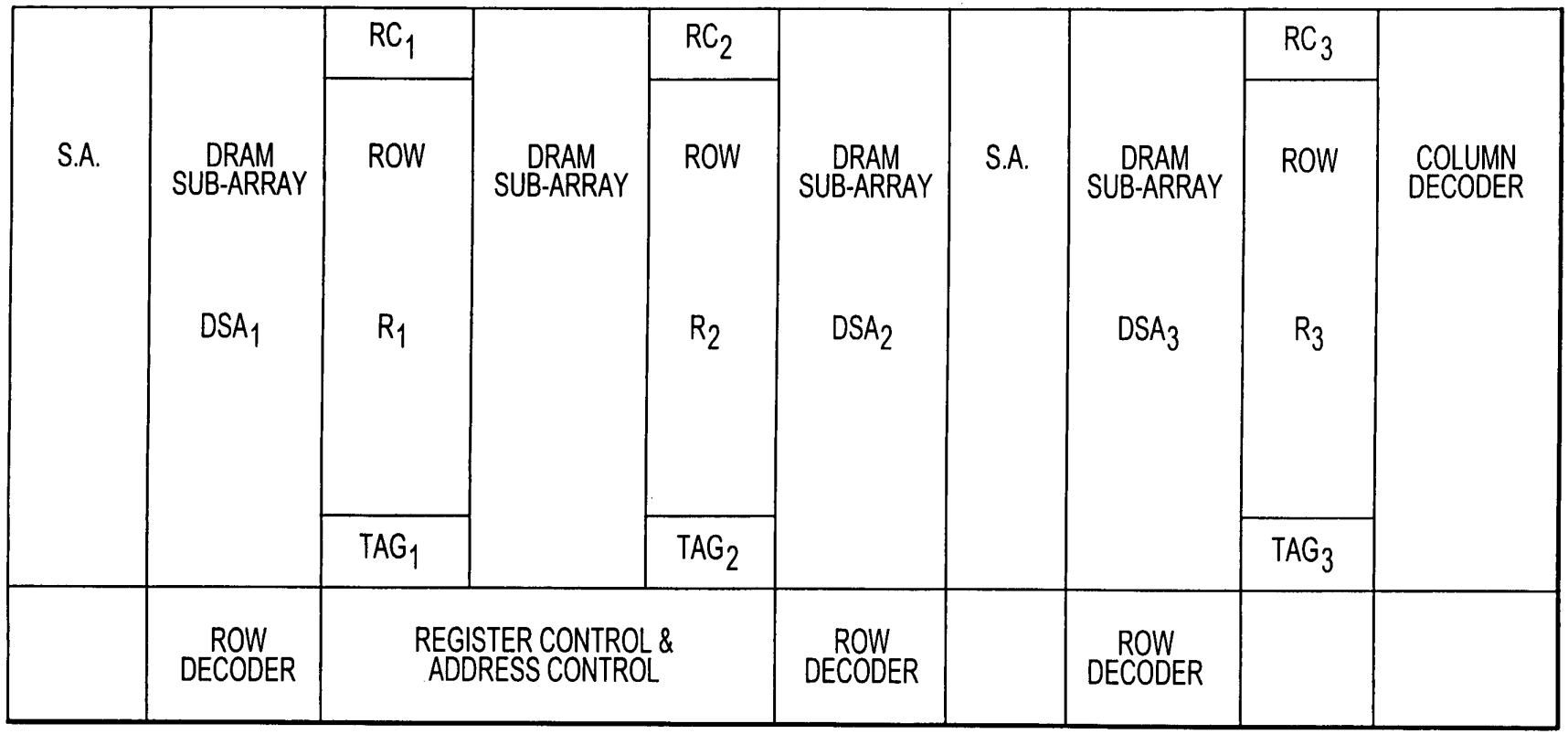
S.A.
DRAM SUB-ARRAY
DSA1
RC1
ROW
R1
TAG1
DRAM SUB-ARRAY
RC2
ROW
R2
TAG2
DRAM SUB-ARRAY
DSA2
S.A.
DRAM SUB-ARRAY
DSA3
RC3
ROW
R3
TAG3
COLUMN DECODER
ROW DECODER
REGISTER CONTROL & ADDRESS CONTROL
ROW DECODER
ROW DECODER

FIG.5

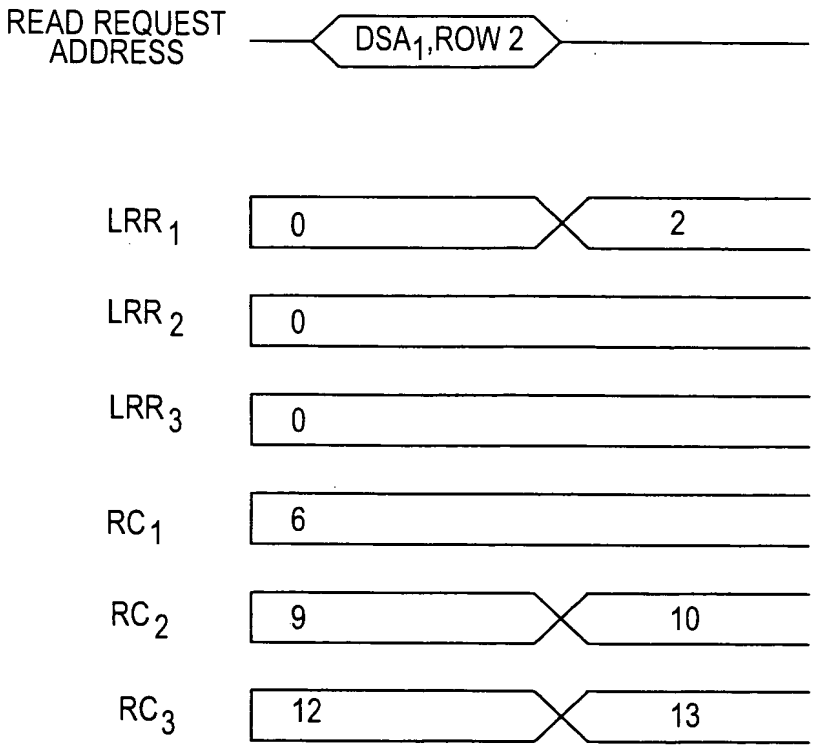
READ REQUEST ADDRESS
DSA1,ROW 2
LRR1
0
2
LRR2
0
LRR3
0
RC1
6
RC2
9
10
RC3
12
13

FIG.6

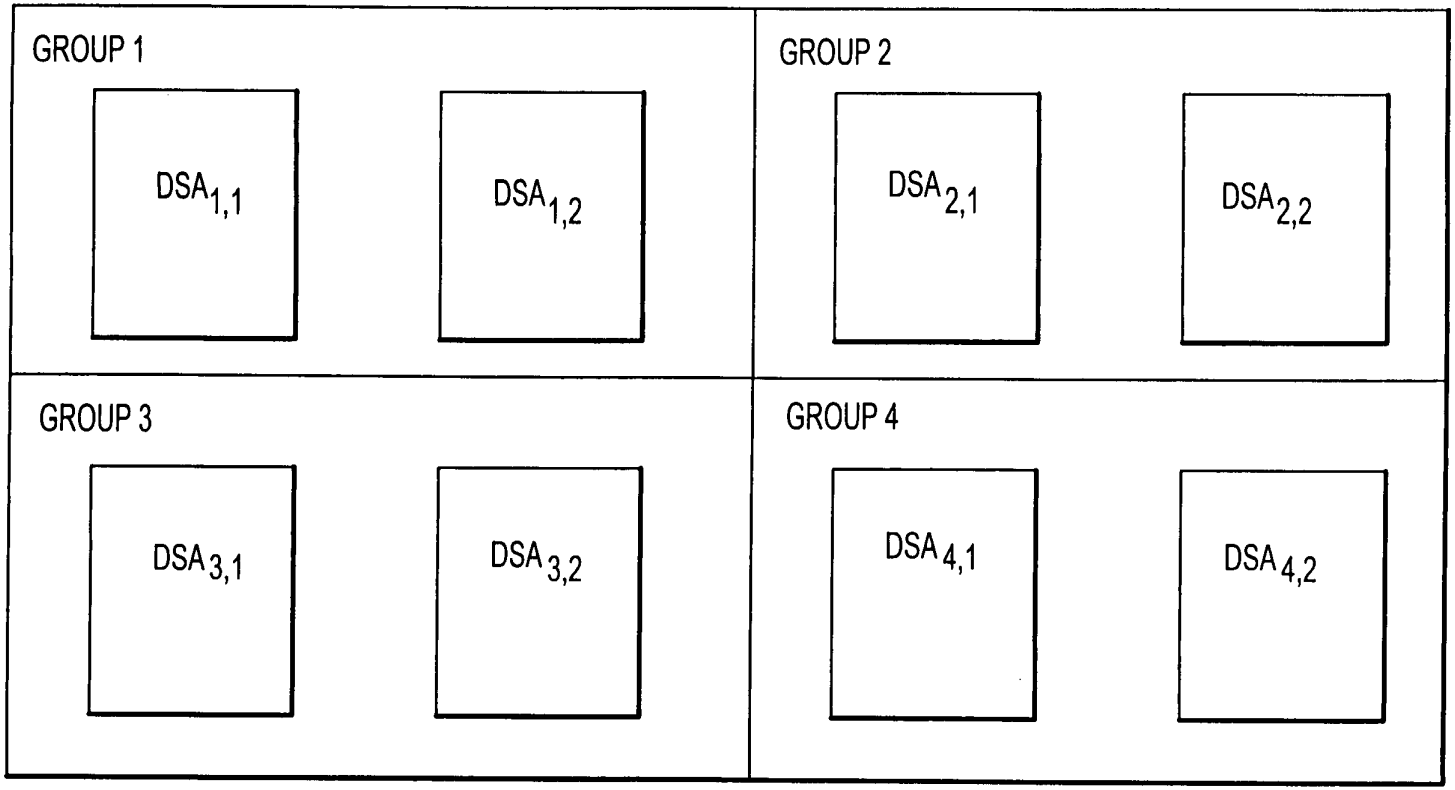

FIG.7

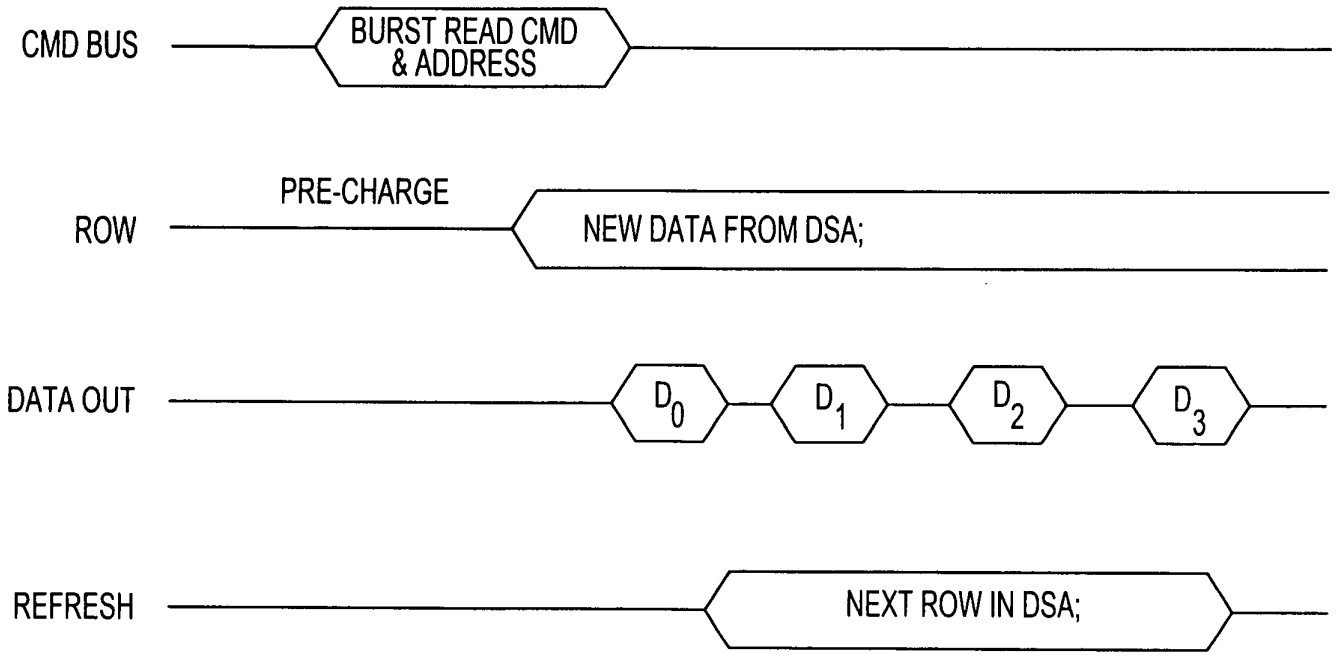
CMD BUS
BURST READ CMD & ADDRESS
ROW
PRE-CHARGE
NEW DATA FROM DSA;
DATA OUT
D0
D1
D2
D3
REFRESH
NEXT ROW IN DSA;

FIG.8